

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0023] with the following amended paragraph:

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Fig. 9 to Fig. 14 are schematic diagrams of a method of forming a liquid crystal on silicon (LCOS) display pixel cell according to the present invention.

10 Fig. 15 is a cross-sectional diagram along line B-B' in Fig. 8.

Please replace paragraph [0026] with the following amended paragraph:

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Please refer to Fig. 9 to Fig. 1[4]5 of schematic diagram of forming the present invention liquid crystal on silicon (LCOS) display pixel cell 246. Fig. 9 to Fig. 14 are cross-sectional diagrams along line A-A' 20 in Fig. 8. Fig. 15 is a cross-sectional diagram along line B-B' in Fig. 8. As shown in Fig. 9, the present invention LCOS display pixel cell 246 is made on a semiconductor wafer 200. The semiconductor wafer 200 comprises a P-type silicon substrate 202. A plurality 25 of isolator 204 are disposed on the surface of the P-type silicon substrate 202 for defining the active area 104 for each device. The isolator 204 is usually a field oxide layer formed by a local oxidation (LOCOS) or a shallow trench isolation (STI).

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Please replace paragraph [0029] with the following

amended paragraph:

In Fig. 9 to Fig. 14, all of the cross-sectional diagrams are drawn along line A-A' in Fig. 8. In order 5 to illustrate the relative sites for sources, drains, and gates more clearly, Fig. 15 is drawn along line B-B' in Fig. 8 such that at least one complete transistor 106 is shown in a cross section. Thereafter, as shown in Fig. 11 and Fig. 15, a photoresist layer (not shown) 10 is utilized and an ion and an ion implantation process is performed to form a source/drain (S/D) 215, 216 of the transistor in the P-type substrate 202 at either side of the transistor gate 214. After that, as shown in Fig. 11, a first dielectric layer 218 is formed on transistor gate 214 and the 15 isolator 204. The first dielectric layer 218 is formed of silicon dioxide by a chemical vapor deposition (CVD) process, a plasma enhanced chemical vapor deposition (PECVD) process, or a process utilizing tetra-ethyl-ortho-silicate (TEOS). Alternatively, the first dielectric layer 218 sometimes is 20 formed with an additional silicon nitride (Si_3N_4) linear underneath by a plasma enhanced chemical vapor deposition (PECVD) process.